GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 770
TO BE ANSWERED ON: 04.02.2026

SECOND PHASE OF DESIGN-LINKED INCENTIVE SCHEME

770. SHRI BHASKAR MURLIDHAR BHAGARE:
DR. AMOL RAMSING KOLHE:
SHRI MOHITE PATIL DHAIRYASHEEL RAJSINH:
PROF. VARSHA EKNATH GAIKWAD:
SMT. SUPRIYA SULE:
SHRI SANJAY DINA PATIL:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) whether the Government is aware of differences between policymakers and industry regarding the structure of the second phase of the Design-Linked Incentive (DLI 2.0) scheme for semiconductor chip design and if so, the details thereof;
(b) whether any assessment has been made of how the proposed pari-passu funding model under DLI 2.0 will impact start-ups and chip design companies in Maharashtra and if so, the details thereof;
(c) whether concerns have been raised that requiring matching private capital may disadvantage smaller firms and early-stage innovators in Maharashtra and if so, the details thereof;
(d) whether the Government proposes any modifications or safeguards to ensure equitable access to DLI 2.0 incentives for semiconductor design companies in Maharashtra and if so, the details thereof; and
(e) whether consultations have been held with industry stakeholders and the Government of Maharashtra to align the DLI framework with the State's semiconductor ecosystem development plans and if so, the details thereof?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (e): Government of India's semiconductor strategy is based on Prime Minister's vision of Make in India and Atmanirbhar Bharat. This is a well thought out strategy to develop manufacturing from finished product assembly, sub-assembly, components, chip design, fabrication, packaging etc.

India's semiconductor design strategy focuses on building a strong, self-reliant chip design ecosystem by leveraging the country's deep talent pool, global design leadership and a growing startup base.

To develop semiconductor manufacturing and to further widen the supply chain ecosystem with respect to manufacturing of active electronics component, Government of India launched Semicon India Program in 2022. Design Linked Incentive Scheme is part of the program. The success of the scheme can be seen from the below performance:

- 24 projects approved for the design of semiconductor chips and SoCs, with a total project value of ₹900 crore, including investments in design infrastructure. These projects address critical sectors such as video surveillance, drone detection, energy metering, microprocessors, satellite communications, and broadband and IoT SoCs.
- 100 fabless chip design companies have been supported with access to advanced chip design infrastructure, cumulatively consuming 55 lakh hours of tool usage.
- 7 chips have been successfully fabricated out of 16 designs taped out across multiple foundries, including advanced nodes such as 12 nm at TSMC.
- 10 patents have been filed, and 140+ reusable semiconductor IP cores developed, serving as critical enablers for advanced chip design.
- 13 companies have raised venture capital funding to scale up and productize their solutions, catalyzing private investment at more than a 3× multiple of the incentives disbursed.

Chips to Startup (C2S) initiative is **aimed at nurturing the semiconductor startup ecosystem by enabling students, researchers and startups to design and develop indigenous chips.** The success of the initiative can be seen from the below performance:

- Advance EDA tools provided to 315 academic institutions and R&D projects initiated at 100 academic institutions.
- 300 training sessions conducted with industry partners
- Over 1 lakh engineering students have enrolled in training with around 67,000 trained in various aspects of chip design.
- 1.6 Crore hours of EDA tools usage by students – World's largest user base of centralized chip design facility.
- 46 institutions across India submitted 122 chip designs for fabrication at the SCL foundry. Of these, 56 student-designed chips were successfully fabricated, packaged, and delivered back to the institutions.
- Over 75 patents filed and development of 100+ chips in progress by these institutions.

Government is committed to further deepen semiconductor design ecosystem. Union Budget 2026-27 has announced the launch of Semicon 2.0.

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