GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 4347
TO BE ANSWERED ON: 18.03.2026

IMPACT OF DLI SCHEME IN MUMBAI

4347. PROF. VARSHA EKNATH GAIKWAD:
SHRI SANJAY DINA PATIL:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) whether the Government is aware that India's semiconductor chip design ecosystem is strengthening under the Design Linked Incentive (DLI) Scheme and the role envisaged for Mumbai as a financial, innovation and startup hub in this ecosystem;
(b) the number of semiconductor chip design startups from Mumbai that have been approved under the DLI Scheme since its inception along with details for the Mumbai Metropolitan Region including Navi Mumbai, sector-wise;
(c) the financial assistance, access to EDA tools, IP cores and technical support extended to Mumbai-based startups under the said Scheme;
(d) whether the Government has assessed the impact of the DLI Scheme in Mumbai on investor confidence, skilled employment generation and commercialisation of chip designs; and
(e) the additional steps proposed to strengthen Mumbai's semiconductor design ecosystem through linkages with universities, incubators, global firms and venture capital networks?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (e): The Government has approved the 'Semicon India Programme' with a total outlay of ₹76,000 crore for the development of a semiconductor and display manufacturing ecosystem in the country.

As part of this, the **'Design Linked Incentive (DLI) Scheme'** has been approved with an outlay of ₹1,000 crore to support domestic companies, startups, and Micro, Small and Medium Enterprises (MSMEs) in semiconductor design.

The DLI Scheme provides for the following support to approved companies:

(a) Design infrastructure support, such as Electronic Design Automation (EDA) tools and Intellectual Property (IP) cores, to help with early prototyping of designs.
(b) Financial incentive of up to 50% of eligible costs, capped at ₹15 Crore per application, for design prototyping, scaling-up, and volume production.
(c) Incentives of 6% to 4% of net sales turnover over five years, capped at ₹30 Crore per application, for deployment & commercialization of chip solutions.

Under DLI Scheme, since its launch in December 2021:

(a) 24 projects approved for the design of semiconductor chips. These projects address critical sectors such as video surveillance, drone detection, energy metering, microprocessors, satellite communications, and broadband and Internet of Things (IoT) SoCs.
(b) 103 fabless chip design companies have been supported with access to advanced chip design infrastructure, cumulatively consuming 60 lakh hours of tool usage.

(c) 7 chips have been successfully fabricated out of 16 designs taped out across multiple foundries, including advanced nodes such as 12 nm at TSMC.
(d) 10 patents filed and 140+ reusable semiconductor IP cores developed, serving as critical enablers for advanced chip design.
(e) 14 companies raised venture capital funding to scale up and productize their solutions.
From Mumbai, Multo Nano Sense Technologies Pvt. Ltd. has been approved under the DLI Scheme for design and development of Microelectromechanical Systems (MEMS) Platform Gas Sensors for Multiple Gases with financial support of ₹14.76 Crore along with access to advanced EDA tools and regular trainings.

It has also raised investment of ₹25.2 Crore from venture capital firms and is closely collaborating with IIT Bombay for design activities.

In addition to above, 2 companies viz. Panache Digilife Limited and Imumbai Semiconductors Pvt. Ltd. have been approved for access to advanced EDA tools for chip design.

The **Chips to Start-up (C2S) Programme** has been initiated for capacity-building across the country with an aim to generate 85,000 number of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design area. So far:

(a) About 68,000 students have been trained under C2S Programme.
(b) Access of advanced chip design tools has been enabled to about 315 institutions across the country with cumulative usage of approximately 200 lakh hours of tool usage.

In order to promote industry-academia collaboration and research and development in chip design area, following 2 academic institutions have been approved from Mumbai for financial support along with access to advanced EDA tools, regular trainings and Multi-project Wafer (MPW) fabrication support under C2S programme:

(a) Indian Institute of Technology (IIT) Bombay has been approved for design and development of Global Navigation Receiver for NAVIC (Navigation with India Constellation) and GPS (Global Positioning System) in collaboration with a startup

The supported project is of the outlay of ₹4.99 Crore for duration of 3 years. Out of this, ₹2.35 Crore has been approved for IIT Bombay. About 1100 students trained at IIT Bombay in chip design area.

(b) Vivekanand Education Society's (VES) Institute of Technology, Chembur has been approved for design and development of chip for Programmable Gain Amplifier (PGA) and reconfigurable Analog to Digital Convertor (ADCs) for wide range of applications with supported project outlay of ₹82.59 Lakh for duration of 3 years. Out of this, ₹74.32 Lakh has been approved for VES.

Two designs for fabrication at SCL foundry have been taped out and about 828 students trained by VES Institute of Technology in chip design area under C2S Programme.

In addition to above, K J Somaiya College of Engineering has been approved for access to advanced EDA tools and regular trainings for chip design. About 525 students trained at K J Somaiya College of Engineering in chip design area.

The DLI Scheme and C2S Programme are pan-India initiatives that have strengthened the semiconductor chip design ecosystem across academia and startups, including in Mumbai, by fostering linkages among universities, startups, and venture capital networks.

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