GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 2879
TO BE ANSWERED ON: 06.08.2025

NIELIT CENTRE OF EXCELLENCE IN CHIP DESIGN

2879. SMT. KAMALJEET SEHRAWAT:
SMT. SMITA UDAY WAGH:
DR. BHOLA SINGH:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) the estimated number of students, researchers and professionals who are expected to benefit annually from the training, research and innovation facilities at the National Institute of Electronics and Information Technology (NIELIT) Centre of Excellence in Chip Design;
(b) the manner in which the Centre is aligned with the objectives of the Government's Make in India initiative and the broader goal of achieving Atmanirbhar Bharat in semiconductor manufacturing and design;
(c) the key programmes and collaborations being facilitated through the Centre to strengthen India's domestic semiconductor ecosystem;
(d) whether NIELIT centre of excellence for chip design is not operational in Delhi-NCR at present;
(e) if so, whether the Government is contemplating to set up such centre in this region;
(f) if so, the time by which it is likely to be set up;
(g) whether the Centre has begun contributing to industry-ready manpower, IP generation or startup incubation in the chip design sector; and
(h) the expected long-term impact of this initiative on improving India's global competitiveness and leadership in the semiconductor and Electronic System Design Manufacturing (ESDM) sector?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (h): The Government of India under the vision of AtmaNirbharta in electronics & semiconductors, is focused on building a complete semiconductor ecosystem including creation of highly skilled workforce.

Chips to Start-up (C2S) is a programme aimed at generating industry-ready manpower specialized in semiconductor chip design, Very Large-Scale Integration (VLSI) and embedded system design. Under this programme, a Skilled Manpower Advanced Research and Training (SMART) Lab has been setup at National Institute of Electronics and Information Technology (NIELIT) Calicut to

enable users to engage with the lab's resources anytime, anywhere for learning and research. More than 65,000 engineers have so far been trained through this initiative.

Further, a Centre of Excellence (CoE) in Chip Design has been set up at Noida in 2023 by NIELIT. It partners with leading semiconductor industries, academic institutions, and startups to strengthen India's chip design ecosystem:

- Focus on faculty upskilling, industry-aligned curriculum, structured internships, and training programs to create industry-ready professionals
- Supports early-stage incubation, facilitates knowledge dissemination and technology transfer

The CoE also conducts a wide range of structured programs for developing industry ready VLSI professionals, including:

- Certification Programs in Application-Specific Integrated Circuits (ASIC) Design, Register Transfer Level (RTL) to Graphic Data System (GDS)-II, Physical Design, and Static Timing Analysis.
- Short-term Courses & Workshops covering VLSI design flow using industry-standard tools.
- Online Programs, including a 6-week internship on RTL to GDS-II and a 42-hour course on VLSI Design Flow.

****