GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 1498
TO BE ANSWERED ON: 04.12.2024

CHIPS TO START-UP PROGRAMME

1498. SHRI B K PARTHASARATHI:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) the details regarding the total number of academic institutions established/ functioning under the Chips to Start-up (C2S) Programme in the country, State-wise;
(b) the number of engineers trained under the said program till date, State-wise;
(c) the total number of SMART Labs established under the C2S programme to impart training in VLSI and Embedded System design areas;
(d) the details of physical and financial progress achieved under the same, State-wise especially in Andhra Pradesh and;
(e) whether the Government has any plan to establish more such SMART Labs in the country; and if so, the details thereof including proposals accepted and under consideration?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (b): Chips to Start-up (C2S) Programme: Chips to Start-up (C2S) Programme is an umbrella programme initiated by Ministry of Electronics and Information Technology (MeitY) with an outlay of Rs. 250 Crore for 5 years in the year 2022 at 113 academic organizations (including 100 academic institutions/ R&D organizations and 13 startups/ MSMEs) spread across the country.

The C2S Programme aims to generate 85,000 number of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design, VLSI (Very Large-Scale Integration) and embedded system design areas and create vibrant fabless chip design ecosystem in the country.

The Programme takes a comprehensive approach by offering students complete hands-on experience in chip design, fabrication, and testing. This is achieved through regular training sessions, conducted in collaboration with industry partners, and by providing mentorship and access to chip design, fabrication & testing resources to students, including state-of-the-art EDA (Electronic Design Automation) tools, access to semiconductor foundries for fabricating their chips etc. These opportunities include implementing the R&D (Research & Development) projects under C2S Programme for development of working prototypes of ASICs (Application-Specific Integrated Circuits), Systems/ SoCs (System-on-Chips), and IP (Intellectual Property) Core designs.

Total 25,257 number of engineering students have been trained at 113 organizations under C2S Programme till date. The State-wise list of 113 organizations via-a-vis number of engineers trained under C2S Programme is at **Annexure-I.**

The EDA (Electronic Design Automation) tools and regular training sessions have been further provided to a total of 240 organizations across the country, including the 113 organizations listed above.

(c) to (e): A**SMART Lab** (Skilled Manpower Advanced Research and Training) has been setup in the year 2022 at NIELIT Calicut under the C2S Programme with an aim to train one lakh engineers nation-wide within 5 years in VLSI and Embedded System design. The 'SMART' remote lab facility is equipped with 200 reconfigurable hardware boards, which can be accessed online 24/7 by students, researchers, and startups across the country. This remote access enables users to engage with the lab's resources anytime, promoting widespread participation in hands-on learning and research. Regular workshops and NSQF (National Skills Qualifications Framework) aligned training programmes are conducted by NIELIT Calicut to impart training to students using SMART lab facility.

Out of the total budget of Rs. 4.00 Crore allocated for 5 years, Rs. 3.40 Crore has been utilized by NIELIT Calicut for SMART Lab activities. Through SMART lab, a total of 42,079 engineers have been trained nationwide, including 6,860 number of engineers from Andhra Pradesh, via training programs conducted using the SMART Lab. The State-wise list of engineers trained via SMART lab is at **Annexure-II.**

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Annexure-I

State-wise list of 113 organizations via-a-vis number of engineers trained under C2S Programme

#	Name of State/ Union territory	Engineering students trained
1.	Telangana	4506
2.	Kerala	2070
3.	Punjab	625
4.	Tamil Nadu	3522
5.	Odisha	1301
6.	West Bengal	821
7.	Uttar Pradesh	1617
8.	Goa	53
9.	Gujrat	289
10.	Karnataka	2497
11.	Madhya Pradesh	1304
12.	Chhattisgarh	158
13.	Himachal Pradesh	369
14.	Bihar	361
15.	Maharashtra	1127
16.	Jharkhand	484
17.	Uttarakhand	944
18.	Rajasthan	302
19.	Haryana	142
20.	Andhra Pradesh	581
21.	Assam	194
22.	Mizoram	26
23.	Manipur	40
24.	Nagaland	78
25.	Tripura	230
26.	Sikkim	128
27.	Arunachal Pradesh	20
28.	Meghalaya	320
29.	Delhi	614
30.	Jammu & Kashmir	101
31.	Chandigarh	274
32.	Puducherry	159
33.	Total	25,257

Annexure-II

State-wise list of engineers trained via SMART lab

#	State/ Union territory	Basic courses on semiconductor design and Embedded system design	Advance courses on semiconductor design and Embedded system design	Engineers trained
1	Andaman and Nicobar Islands	6	0	6
2	Andhra Pradesh	6793	67	6860
3	Arunachal Pradesh	47	2	49
4	Assam	263	3	266
5	Bihar	514	6	520
6	Chandigarh	44	2	46
7	Chhattisgarh	217	8	225
8	Daman and Diu	9	0	9
9	Delhi	778	14	792
10	Goa	41	0	41
11	Gujarat	513	18	531
12	Haryana	508	12	520
13	Himachal Pradesh	81	1	82
14	Jammu and Kashmir	250	2	252
15	Jharkhand	265	3	268
16	Karnataka	4464	95	4559
17	Kerala	4068	158	4226
18	Ladakh	2	0	2
19	Madhya Pradesh	1169	23	1192
20	Maharashtra	3945	83	4028
21	Manipur	251	0	251
22	Meghalaya	51	2	53
23	Mizoram	16	3	19
24	Nagaland	5	2	7
25	Odisha	1066	26	1092
26	Puducherry	573	12	585
27	Punjab	417	9	426
28	Rajasthan	552	10	562
29	Sikkim	26	1	27
30	Tamil Nadu	7258	128	7386
31	Telangana	3018	51	3069
32	Tripura	54	1	55
33	Uttar Pradesh	2818	28	2846
34	Uttarakhand	175	4	179
35	West Bengal	1024	24	1048
	Total	41281	798	
	Grand Total	42,079		

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