GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 1460
TO BE ANSWERED ON: 04.12.2024

ENCOURAGING INNOVATIONS FOR CHIPS

1460. SHRI S JAGATHRATCHAKAN:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) whether the Government concurs with the view that the country needs to encourage innovations that cater to the ever-increasing demands for faster, cheaper and more powerful chips which includes providing greater funding to startups and private research institutions much like the way US offers grants for projects that can create tremendous value for society; and
(b) if so, the steps taken/being taken by the Government in this regard and if not, the reasons therefor?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) and (b): Government is focused on its objective of building the overall semiconductor design and manufacturing ecosystem with an emphasis on fostering research and innovation within the country. To achieve this, several initiatives are taken, including the establishment of R&D (Research & Development) and manufacturing infrastructure, capacity-building initiatives, and skill development programs to address workforce gaps. The government also supports R&D initiatives for advancing technology and provides incentives to startups & private research institutions, encouraging them to create innovative solutions, in areas like semiconductor chip design, to address societal requirements. Some of these initiatives of Government of India include, but are not limited to the following:

(i) Generating industry-ready manpower in chip design: Chips to Start-up (C2S) Programme is an umbrella capacity building programme initiated by Ministry of Electronics and Information Technology (MeitY) with an outlay of Rs. 250 Crore for 5 years in the year 2022 at 113 academic organizations (including 100 academic institutions/ R&D organizations and 13 startups/ MSMEs) spread across the country.

The C2S Programme aims to generate 85,000 number of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design, VLSI (Very Large-Scale Integration) and embedded system design areas and create vibrant fabless chip design ecosystem in the country.

The C2S Programme takes a comprehensive approach by offering students complete hands-on experience in chip design, fabrication, and testing. This is achieved through regular training sessions, conducted in collaboration with industry partners, and by providing mentorship and access to chip design, fabrication & testing resources to students including state-of-the-art EDA (Electronic Design Automation) tools, access to semiconductor foundries for fabricating their chips etc. These opportunities include implementing the R&D (Research & Development) projects under C2S Programme for development of working prototypes of ASICs (Application-Specific Integrated Circuits), Systems/ SoCs (System-on-Chips), and IP (Intellectual Property) Core designs.

(ii) Supporting semiconductor research & innovation ecosystem: MeitY supports R&D projects for design & development of semiconductor chips tailored for strategic &

societal needs at academic institutions, research organizations, and startup companies. Some of these initiatives includes but not limited to the following- design, development, and fabrication of a range of 32-bit/64-bit multi-core microprocessors, chipsets for NavIC (Navigation with Indian Constellation) receivers, and Digital Programmable Hearing Aids (DPHA) using indigenous processors, Photonics/ Quantum Chips, among other applications. These initiatives have also resulted in generating start-ups in chip design area.

(iii) Catalysing semiconductor design and manufacturing industry: Government of India has approved the 'Modified Programme for Semiconductors and Display Fab Ecosystem' with an outlay of ₹76,000 crore in order to catalyse the semiconductor & display ecosystem in the country. The Design Linked Incentive (DLI) Scheme has been approved as part of it with an outlay of Rs. 1000 Crore to offset the disabilities in the domestic semiconductor chip design industry as well as move up in value-chain and strengthen the semiconductor chip design ecosystem in the country.

The DLI Scheme offers financial incentives & design infrastructure support to domestic companies, start-ups and MSMEs across various stages of development & deployment of semiconductor chips.

42 design companies (including start-ups and MSMEs) have been approved for design infrastructure support under the DLI Scheme. Out of these, 15 companies have also been approved for financial support for developing semiconductor chip/ SoCs for applications in sectors such as automotive, mobility, computing, communications etc.

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