GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO.1548
TO BE ANSWERED ON: 31.07.2024

GREENFIELD SEMICONDUCTOR FAB

1548. DR.SANJAY JAISWAL:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGYbe pleased to state:

(a) whether the Government is aware of the details of major objectives to develop research and development and design capabilities for setting up of greenfield semiconductor fab and display fab in the country;
(b) if so, the details thereof;
(c) the details of incentives given for production of semiconductor and display in India; and
(d) the categories of assistance provided under Design Linked Incentive (DLI) scheme?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (d):Government is very focused on its objective of building the overall semiconductor ecosystem and ensure that, it in-turn catalyses India's rapidly expanding electronics manufacturing and innovation ecosystem. As a part of Semicon India Programme, the Union Cabinet has approved the Design Linked Incentive (DLI) Scheme with an aim to offer the fiscal support as well as design infrastructure support to domestic companies, start-ups and MSMEs across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design over a period of 5 years.Following support is provided to approved companies under the Design Linked Incentive (DLI) Scheme:

(i) **Fiscal support:**
   a. **Product Design Linked Incentive-** Reimbursement of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application.
   b. **Deployment Linked Incentive-** Reimbursement of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application.

(ii) **Design Infrastructure support:**Access to design infrastructure such as EDA Tools, IP Cores and support for prototyping the designs in MPW (Multi Project Wafer) and post-silicon validation support, to the approved applicants for designing the semiconductor chips.

Under the Chips to Startup (C2S) Programme being implemented at 113 academic institutions/ R&D organizations/ Start-ups/ MSMEs, 85,000 number of high-quality and qualified engineers are being trained in several areas. These include Very large-scale integration (VLSI) and Embedded System Design as well as development of 175 ASICs (Application Specific Integrated Circuits), working prototypes of 20 System on Chips (SoC), 30 FPGA based designs and 30 IP Cores over a period of 5 years.

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