GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 1454
TO BE ANSWERED ON: 10.02.2021

MANUFACTURING OF CHIP

1454. SHRI KUNWAR PUSHPENDRA SINGH CHANDEL:
SHRIMATI MALARAJYA LAXMI SHAH:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) whether the Government has formulated any special incentive policy for the indigenous manufacturing of electronic chip, mobile chip and computer processor;
(b) if so, the details thereof; and
(c) the details of investment made for manufacturing of these electronic products in the country during the last three years; State/UT-wise?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI SANJAY DHOTRE)

(a) and (b): Government offered special incentives for setting up of Semiconductor Wafer Fabrication (FAB) Facilities in India. The main incentives offered are **Annexed**. Government had earlier approved two proposals for setting up of Semiconductor FAB facility in India - one from the consortium led by M/s. HSMC Technologies India Pvt. Ltd. and the other from consortium led by M/s. Jaiprakash Associates Ltd. Letter of Intent (LoI) dated 19.03.2014 was issued to both the consortia. As per the LoI, both the consortia were required to submit certain documents for demonstration of commitment. The consortium led by M/s. Jaiprakash Associates Ltd. withdrew their proposal on 02.03.2016 and the consortium led by M/s. HSMC Technologies India Pvt. Ltd. could not submit the requisite documents for demonstration of commitment, despite being provided extension of time on several occasions. Hence, the LoI issued to M/s. HSMC Technologies India Pvt. Ltd. was cancelled on 20.04.2018. Therefore, both the proposals for setting up of semiconductor FAB facilities in the country could not materialize.

(c): Does not arise.

****

Annexure

Following main incentives were offered in 2014 for Setting up of Semiconductor Wafer Fabrication (FAB) Facility in India:

a. 25% subsidy on capital expenditure and tax reimbursement as admissible under Modified Special Incentive Package Scheme (M-SIPS) Policy. Disbursement under MSIPS to be made pari passu on a quarterly basis as against the annual basis as envisaged in the M-SIPS Policy.

b. Investment linked deduction under Section 35AD of the IT Act.

c. Viability Gap Funding in the form of Interest free loan to be capped at 20% of the capital expenditure (as admissible under M-SIPS)

d. Exemption of Basic Customs Duty (BCD) for non-covered capital items

e. Reimbursement of Countervailing Duty (CVD) on purchase of capital goods as admissible under M-SIPS Policy.

f. Reimbursement of Excise duty paid on the products of the FAB for a period of 10 years.

g. Deduction on expenditure on R&D as admissible under Section 35(2AB) of the Income Tax (IT) Act

h. Reimbursement of expenditure to be incurred for the training of the project personnel as applicable under National Skills Development Corporation (NSDC) Scheme.

****