GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 5458
TO BE ANSWERED ON: 05.04.2023

FUNDING OF SEMI-CONDUCTOR MATERIALS RESEARCH

5458. SHRI T.R BAALU:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) whether the Government is planning to fund new semi-conductor materials research, new design architectures for critical equipment, intellectual property protection, and technical standards;
(b) if so, the details thereof; and
(c) the initiatives that have been taken/proposed to be taken by the Government keeping in view that India is a global hub for chip design and design services?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI RAJEEV CHANDRASEKHAR)

(a) and (b): Yes Sir. Research in semiconductors including materials is a critical part of Government's policy in developing an overall semiconductor ecosystem in the country. Government is committed to develop an overall semiconductor ecosystem in the country to catalyse India's rapidly expanding electronics manufacturing and innovation ecosystem.

Ministry of Electronics and Information Technology (MeitY) is financially supporting to develop emerging semiconductor materials for Semiconductor Photonic Integrated Circuits (PICs); which has varied applications including Aerospace and Defence, Datacom, IoT, Quantum Technologies etc. Some of the R&D projects initiated in this direction are as following:

(i) An R&D project entitled **"Centre for Programmable Photonic Integrated Circuit and Systems (CPPICS)"**is being implemented at Indian Institute of Technology Madrassince December 2020 in collaboration with industry (M/s Si2 Microsystems, Bangalore) to design, manufacture and develop applications based on Field programmable photonic gate array (FPPGA) core technology and its applications using Silicon Photonics Platform.
(ii) Another R&D project entitled **"National Centre for Quantum Material Technologies (NCQMT)"**is being implementedat Centre for Materials for Electronics Technology (C-MET), Punesince March 2022 aiming to develop quantum material technology on Diamond Substrates.The centre is engaged in establishing ISO17025 standard lab and its infrastructure. NCQMT has signed MOU with M/s Hind HiVacuum Company Pvt. Ltd, Bangalore for co-development of Diamond Substrate manufacturing process and machines (Microwave Plasma Enhanced Chemical Vapor Deposition(MPECVD));and aims to develop Indiansupply chain for the global market.
IP rights for aforementioned technologies will be protected through national and international patents in due course.

(c): Yes Sir. Government is cognizant of the fact that India is a global hub for chip design and design services. With thousands of chips designed every year by an exceptional design talent pool making up to 20% of world's semiconductor design engineers in the country, India

remains a highly attractive destination for global semiconductor companies with most of the major semiconductor companies present in the country.

Ministry of Electronics and Information Technology has initiated a number of dedicated schemes and programmes to increase the domestic share in chip design area and create vibrant domestic chip design industry in the country.

(i) **Semicon India programme:** has been initiated by Government with anoverall outlay of Rs. 76,000 Crore for development of semiconductor and display manufacturing ecosystem in the country.As Research & Development (R&D) is the foundation for the developing semiconductor ecosystem in the country, up to 2.5 % of the total outlay of the Semicon India programmeis allocated to the R&D, Skill Development and Training requirements for developing semiconductor ecosystem in India.

(ii) **'Semicon India Future Design: Design Linked Incentive (DLI) Scheme'**offers financial incentives and design infrastructure support across various stages of development and deployment of semiconductor designs for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design. The DLI Scheme provides "Product Design Linked Incentive" of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application and "Deployment Linked Incentive" of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application. Out of 23 applications receivedfrom the domestic companies under the DLI Scheme, 3 applicants have been granted approval; while other applications are being evaluated for support under the DLI Scheme.

(iii) **Chips to Start-up (C2S) Programme:** aims to generate 85,000 number of industry-ready manpower at B.Tech, M.Tech& PhD level specialized in the area of VLSI/ Chip and Embedded System Design over a period of 5 years at academia, R&D organizations, start-up and MSME across the country.
'ChipIN Centre' has been setup at C-DAC Bangalore, as a one-stop support centre, for providing services for chip design and fabrication; including access to state-of-the-art chip design tools, Multi-project Wafer fabrication services etc.104 organizations across the country (including 91 Academia/ R&D Organizations and 13 Startup/ MSMEs) have been selected for providing support for designing chips in varied application areas under C2S Programme.

(iv) As a step towards meeting India's future requirements ofstrategic&industrial sectors including that of automotive, mobility and computing sectors, following programmes have been initiated by MeitY:

(a) An R&D project entitled "**Microprocessor Development Programme"** is being implemented at IIT Madras, C-DACand IIT Bombay which aims to design and developfamily of 32-bit and 64-bit, multi-core microprocessors using open-source ISA (Instruction Set Architecture).32-bit/ 64-bit variants of SHAKTI, VEGA and AJIT Microprocessors have been designed and fabricated by IIT Madras, C-DAC and IIT Bombay under Microprocessor DevelopmentProgramme.

(b) A project fordesign, development and deployment of Integrated NavIC and GPS Receiveris being implemented by domestic companies; wherein the integrated NavIC and GPSChipsets designed and fabricated by M/s Accord Software and Systems has been qualified by SAC(ISRO) for deployment in civilian sector in the country.

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