GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
RAJYA SABHA
UNSTARRED QUESTION NO. 708
TO BE ANSWERED ON: 05.12.2025

PROMOTION OF CHIPSET PACKAGING, TESTING AND ASSEMBLY

708. SHRI KARTIKEYA SHARMA:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be pleased to state:

(a) the initiatives for promotion of chipset packaging testing and assembly in the country, the details thereof;
(b) whether the Ministry is running any initiatives to support entrepreneurship and MSMEs working in the domain;
(c) the strategy of the Ministry to provide preference in terms of work orders to such establishments so that they have healthy revenue;
(d) whether the Ministry has planned any IP pool and research support for new age ventures in the electronics packaging, assemble and testing domain; and
(e) the details of financial support, loan and professional guidance being provided by the Ministry?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI JITIN PRASADA)

(a) to (e): The Government attaches a high priority for the semiconductor sector as it is a foundational industry for the economy and also plays a critical role in making India Atma Nirbhar in electronic manufacturing. To achieve resilience in supply chain of electronics manufacturing, government provides fiscal support through Semicon India programme for settting up of semiconductor fabs, display fabs, and ATMP (assembly, testing, marking and packaging) units.

Under Semicon India programme, the Government provides **f**iscal support of 50% of the Capital Expenditure on *pari-passu* basis for setting up of Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / Outsourced Semiconductor Assembly and Test (OSAT) facilities in India.

MSMEs & Start ups are also eligible to apply for the project for ATMP/OSAT facilities as the scheme doesn't provide for any revenue threshold criteria for the applicant. Apart from above, MSMEs would also benefit from being part of the supply chain of the approved applicants under Semicon India Programme.

Further, start-ups and MSMEs can also benefit from 'Design Linked Incentive (DLI) Scheme by availing fiscal support for design, development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores.

It also provides infrastructure support for chip design to eligible applicants which include EDA tools, IP cores and fabrication support etc. Under this scheme, fiscal support has been approved for 24 proposals to design chips and SoCs for applications. Apart from above, infrastructure support like EDA tools for designing the chips are also being provided to 91 startups.

******