GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
RAJYA SABHA
UNSTARRED QUESTION NO. 1047
TO BE ANSWERED ON: 28.07.2023

PROMOTION OF DESIGN AND R&D IN SEMI-CONDUCTOR INDUSTRY

1047. SHRI V. VIJAYASAI REDDY:

Will the Minister of Electronics and Information Technology be pleased to state:

(a) whether Government has taken any initiatives to promote design and R&D in the semi-conductor industry;
(b) if so, the details thereof and if not, the reasons therefor;
(c) whether Government also intends to provide support to the industry in areas of display fab, packaging and testing facilities, and chip design centres; and
(d) if so, the details thereof and if not, the reasons therefor?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI RAJEEV CHANDRASEKHAR)

(a) to (d): Government is focused on its objective of catalysing overall semiconductor ecosystem to further expand India's already rapidly expanding electronics manufacturing and innovation ecosystem. Government has approved the Semicon India programme with a total outlay of INR 76,000 crore for the development of semiconductor and display manufacturing ecosystem in the country. Under the Semicon India programme, upto 2.5% of the outlay of the schemes have been earmarked for meeting the R&D, skill development and training requirements for the development of semiconductor and display ecosystem in India. The programme aims to provide financial support to companies investing in semiconductors, display manufacturing and design ecosystem. This will pave the way for India's growing presence in the global electronics value chains.

Following four schemes have been introduced under the aforesaid programme:

i. '**Modified Scheme for setting up of Semiconductor Fabs in India**' for attracting large investments for setting up semiconductor wafer fabrication facilities in the country to strengthen the electronics manufacturing ecosystem and help establish a trusted value chain. The Scheme extends a fiscal support of 50% of the project cost on *pari-passu* basis for setting up of Silicon CMOS based Semiconductor Fab in India.
ii. '**Modified Scheme for setting up of Display Fabs in India**' for attracting large investments for manufacturing TFT LCD or AMOLED based display panels in the country to strengthen the electronics manufacturing ecosystem. Scheme extends fiscal support of 50% of Project Cost on *pari-passu* basis for setting up of Display Fabs in India.
iii. '**Modified Scheme for setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab / Discrete Semiconductors Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP) / OSAT facilities in India'** extends a fiscal support of 50% of the Capital Expenditure on Pari-passu basis for setting up of Compound Semiconductors / Silicon Photonics (SiPh) / Sensors (including MEMS) Fab/ Discrete Semiconductor Fab and Semiconductor ATMP / OSAT facilities in India.

iv. **'Semicon India Future Design: Design Linked Incentive (DLI) Scheme'**offers financial incentives, design infrastructure support across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design. The scheme provides "Product Design Linked Incentive" of up to 50% of the eligible expenditure subject to a ceiling of ₹15 Crore per application and "Deployment Linked Incentive" of 6% to 4% of net sales turnover over 5 years subject to a ceiling of ₹30 Crore per application.

Further, Semicon India Future Skills / Chip to Startup (C2S) Programme has been initiated to create 85,000 number of highly qualified global talent over a period of 5 years.
Additionally, a R&D Committee has been constituted comprising of representatives from global semiconductor Industry, Academia and Government to create a roadmap for semiconductor R&D in India.

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