GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
RAJYA SABHA
UNSTARRED QUESTION NO. 694
TO BE ANSWERED ON: 08.02.2019

NATIONAL SUPERCOMPUTING MISSION

694. DR. T. SUBBARAMI REDDY:

Will the Minister of Electronics & Information Technology be pleased to state:-

(a) the broad aims and objectives of National Supercomputing Mission(NSM);
(b) by when supercomputers being built by Centre for Development of Advanced Computing (C-DAC) would be ready;
(c) the basic features of these supercomputers and where would they be deployed; and
(d) the total cost of developing these supercomputers and the percentage of indigenous technology being used therein?

ANSWER

MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI S.S. AHLUWALIA)

(a): Cabinet Committee on Economic Affairs (CCEA) has approved the NSM on 27th March, 2015. The mission is to be jointly implemented by MeitY and DST along with C-DAC and IISc as the executing agencies with a total estimated cost of Rs 4,500.00 Crores over a period of Seven Years. Contribution of MeitY would be Rs 1,760 Crore and contribution of DST would be Rs 2740 Crore.

Key Deliverables of the Mission:

- Creation of NSM facilities and infrastructure (50% Build 50% Buy)
  - Entry level supercomputers (5 to 15 TF in ~50 centres)
  - Midrange supercomputers (200-500 TF in 20 zonal centres)
  - Large supercomputers (2-8 PF in 3 nodal centres)
  - Million core cloud infrastructure (One) with 25-30 Petabytes of storage
  - National Supercomputing Grid by interconnecting various HPC systems over National Knowledge Network (NKN)
- R&D leading to next generation Exascale computing readiness
- HPC applications in at least 5 major areas
- Human Resource Development (~ 20,000 trained professionals to handle and spearhead HPC activities)

(b): Under Build approach, C-DAC is building systems in a phased manner
Phase-I (Assembled in India):

Components (Motherboard, Chasis etc.) of sub-systems (Compute nodes, Network switches etc.) would be imported and assembled in India by the successful bidder.

Phase-II (Manufactured in India):

Components of sub-systems would be manufactured in India by local EMS vendors and assembled by the successful bidder. The design IP of the sub-systems would still be owned by bidder.

Phase-III (Designed and Manufactured in India):

Design of sub-systems would be done by CDAC, manufactured by local EMS vendors and assembled by CDAC/Indian Industry partners.

In Phase-I, three systems are planned to be installed by C-DAC by April 2019.

(c): The compute capacities of the supercomputers and the locations where they would be deployed under Phase-I are as below:

IIT Kharagpur:	1.3 PF (Peta Flops)
IIT Varanasi:	650 TF (Tera Flops)
IISER Pune:	650 TF

(1PF= 10^{15} Flops, 1TF= 10^{12} Flops)

(d): The total cost of the above three machines being built under Phase-I is Rs 95.00 Crore plus GST at actual.

The complete system software stack indigenously developed by C-DAC for all three phases. The percentage of indigenous technology by the end of Phase-III would be 40%.

****